

REMARKS

Claims 1-10 are pending in the present application. Claims 1 and 4 are independent. Claims 7 and 8 are amended.

Drawings

The drawings have been objected to under 37 C.F.R. § 1.83(a). As suggested by the Examiner, Figures 1A-1E and 2A-2E have been amended to include a substrate and are transmitted with a Drawing Change Authorization Request accompanying this Amendment. Accordingly, Applicant requests this objection be withdrawn.

Claim Objections

Claims 7 and 8 have been objected to due to minor informalities. As per the Examiner's comments, claims 7 and 8 have been amended. Applicant notes that this Amendment does not further narrow the claims and is not in response to prior art. Accordingly, Applicant requests that this objection be withdrawn.

Claim Rejections

Claims 1-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (1A-1E) in view of Kadomura (U.S. Patent No. 5,230,772). Applicant respectfully traverses this rejection.

In formulating this rejection, the Examiner has interpreted the "Related Art" discussed in the Specification on pages 2-3 and depicted in Figures 1A-1E as admitted "Prior Art". However, the Specification does not refer to the "Related Art" as "Prior Art" and Applicant has not admitted that the material designated as "Related Art" is "Prior Art".

"Prior Art" is a term specifically designated to identify material which is known to be statutory prior art to the invention. However, if it is not clear whether such material is statutory prior art, then the use of the phrase "Prior Art" in the drawing figures would not be proper, and a label such as "Related Art", as used by Applicant, would be more appropriate. If Applicant was aware that the materials referred to as "Related Art" were actually "Prior Art", then Applicant would have referred to the "Related Art" as "Prior Art". Since Applicant has not admitted any "Prior Art", this rejection is improper.

Even assuming *arguendo* that Applicant's specification does contain "Prior Art" (which Applicant does not admit), the "Related Art" and Kadomura, either alone or in combination, do not teach all the features of independent claims 1 and 4.

As admitted by the Examiner, the Related Art fails to disclose, "removing the photoresist using an etching gas that is non-reactive with respect to the lower electrode," as recited in part by claim 1 and similarly claim 4. See Office Action pg. 3, lines 20-22 and pg. 5, lines 10-12.

To make up for this deficiency, the Examiner inappropriately relies on Kadomura. Kadomura discloses a dry etching method to prevent the effects of micro loading that result from patterning a photoresist deposited on a substrate. Kadomura contends that the dry etch process will prevent many of the problems of other etch techniques, such as over etching the substrate due to non-uniform etch rates of the photoresist layer.

Although Kadomura discloses the dry etch process for patterning photoresist that has been deposited on a substrate, Kadomura provides not teachings or suggestions of applying the dry etch technique to remove photoresist deposited on an electrode material rather than on the substrate. Therefore, Kadomura does not disclose the above quoted features of claims 1 and 4 and does make up for the deficiencies of the related art.

Accordingly, claims 1 and 4 are allowable over the prior art. Regarding dependent claims, 2, 3 and 5-10, these claims are allowable for at least the same reasons as their corresponding independent claims. Therefore, Applicant respectfully requests removal of this rejection.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the rejection and allowance of claims 1-10 is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

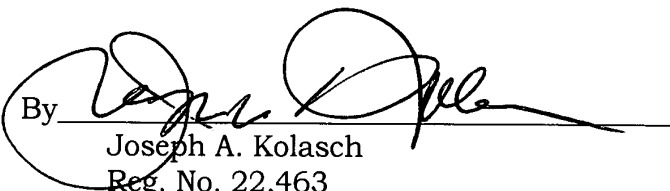
If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to contact the Jayne Saydah (Reg. No. 48,796) at (703) 205-8000, in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By


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Attachment: Version With Markings Showing Changes Made

VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE SPECIFICATION

The paragraph starting on page 2, line 5 has been replaced with the following rewritten paragraph.

A gate oxide film and a gate electrode are sequentially formed on some region of a semiconductor substrate 10, and source and drain regions are formed in the semiconductor substrate 10 at both sides of the gate electrode (not shown).

The paragraph starting on page 6, line 1 has been replaced with the following rewritten paragraph.

The method for fabricating a capacitor of a semiconductor device according to the present invention is performed in such a manner that a conductive layer is deposited on a semiconductor substrate [(not shown)] 110. A photoresist pattern is then formed on the conductive layer, and the conductive layer is etched using the photoresist as a mask to form a lower electrode. The photoresist is then removed using an etching gas having no volatility with respect to the lower electrode, and a dielectric film and an upper electrode are thereafter sequentially formed on a surface of the lower electrode.

The paragraph starting on page 6, line 17 has been replaced with the following rewritten paragraph.

A gate oxide film and a gate electrode are sequentially formed on a region of a semiconductor substrate 110, and source and drain regions are formed in the semiconductor substrate 110 at both sides of the gate electrode (not shown).

The paragraph starting on page 6, line 22 and ending on page 7, has been replaced with the following rewritten paragraph.

A conductive material such as polysilicon or tungsten, or another conductive material having low resistance is then deposited on the interleaving insulating film 101 [includingin] including in the contact hole. A contact plug 102 is formed within the contact hole by an etch-back process or a chemical mechanical polishing process so that the conductive material is only formed within the contact hole.

IN THE CLAIMS

The claims have been amended as follows.

7. (Amended) The method of claim 4, wherein the insulating film patterns comprise[s] an oxide film.

8. (Amended) The method of claim 4, wherein the insulating film patterns [is] are formed by stacking two insulating films.